A 10 Gb/s Package For Digital ICs

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Abstract—**Experimental research prototype packages with 26 10 Gb/s I/O ports were designed for two GaAs telecom ICs. The prototypes are based upon a commercially available ceramic microwave package with an exterior size of 0.450" square, and an interior cavity size of 0.250" square. The copper-tungsten base provides excellent heat dissipation and rigidity while providing a close thermal expansion match to GaAs. A 5 mil alumina substrate is used to carry microstrip transmission line circuits from the package edge to the die mounted at the package center. A low-inductance ground ring surrounds the die cavity in the package to provide flexible low-noise grounding of the die without compromising signal integrity on the high-speed lines. Measurements show the package has usable bandwidth to 35 GHz and crosstalk is better than −35 dB for adjacent high-speed signal paths. The results demonstrate that packaging need not be the limiting factor for complex high-speed digital integrated circuits.**

I. Introduction

This paper presents two experimental research prototype chip-carriers for packaging 10 Gb/s SONET STS-192 multiplexing, framing, and phase aligner Heterojunction Bipolar Technology (HBT) integrated circuits [1]. The chip carriers and ICs were developed as part of the work of the SONET/ATM Self-Healing Ring Consortium (Bell Communications Research, Inc., Rockwell International Corporation, Lucent Technologies, Inc., Southwestern Bell Technology Resources, Inc., Tektronix,Inc., and Washington University in St. Louis). The consortium is conducting a 10 Gb/s SONET/ATM self-healing ring research and development project†. One of the initial tasks of the project is to prototype experimentally the key enabling optical and electronic subsystems for the 10 Gb/s SONET physical layer.

Packaging both the 10 Gb/s multiplexer-phase aligner and demultiplexer-framer ICs represents a significant challenge because of the combination of high-speed signals and a large signal count (26 high-speed (>1.25 Gb/s) and 20 low-speed (<1 MHz) signals for the demultiplexer, and 26 high-speed and 21 low-speed signals for the multiplexer). To maintain signal integrity at STS-192 rates, microwave techniques must be employed to control signal reflections, dispersion, and cross-talk along the signal path from the IC to the outside circuitry. Thermal management is also critical because each AlGaAs/GaAs HBT integrated circuit dissipates approximately 3 W of power. In addition, care must be taken to ensure that package parasitics are minimized, and package resonance does not occur within the energy bandwidth of the expected signals, in this case up to at least 20 GHz.

This research was supported by the Defense Advanced Research Projects Agency under the Technology Reinvestment Project (TRP) Defense Dual Use Critical Technology Partnership Program.

† http://www.arl.wustl.edu/arl/projects/trp/oc192trp.html

II. Package Design

A ceramic package was used with an exterior size of 0.450" square, and an interior cavity size of 0.250" square. The prototype package is based upon a commercially available SEC-580234 patented ceramic microwave package from the StratEdge Corporation [2]. This standard package was modified to increase its high-speed I/O count from the original

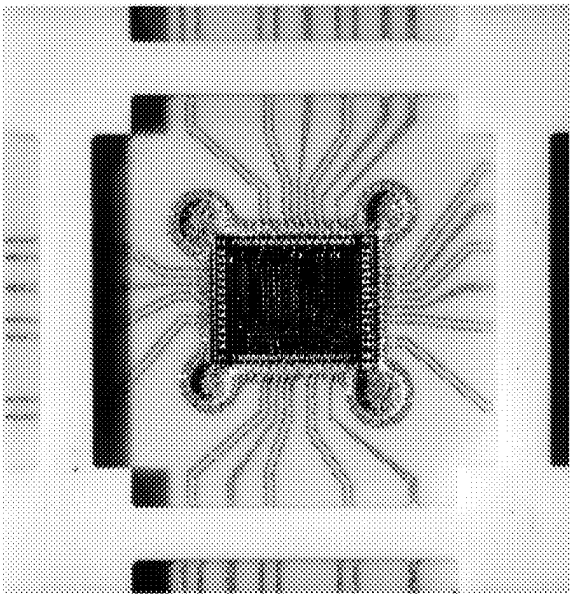

Figure 1. Photograph of the 10 Gb/s multiplexer chip carrier. The package is 0.450 inches square and the GaAs HBT die is 3 × 2 mm square. A ceramic seal ring at the package periphery isolates the interior chamber which houses the die. A custom transition was designed for the signal trace where it passes through the seal ring. The signal lead bond wires are jumpered over the ground ring surrounding the die. At each corner of the ground ring a large via to the package base is visible.

two leads to the 26 leads required in this application. In addition, an extensive redesign of the internal cavity of the package was made to provide a low-inductance ground ring around the periphery of the die to allow ground connections to the die at any point on its perimeter (Fig. 1). Packages with these custom modifications were fabricated by StratEdge for Bellcore.

The package in its original unmodified form provides resonance free operation from dc to over 35 GHz. The tungsten-copper base provides excellent heat dissipation (150 W/mK) and rigidity, as well as a good coefficient of thermal expansion match to GaAs. A 5 mil alumina substrate is used to support the transmission-line circuits from the package edge to the die mounted at the package center. A precision hole is laser cut into the alumina substrate to form a well that the die sits in. The hole permits the die to be attached directly to the tungsten-copper base underneath the substrate for optimum thermal conductivity between the die and external heatsink, and simplifies die alignment during assembly. Additionally, this arrangement allows the transmission lines to be brought up to within 4 mil of the die on all four sides. This facilitates maintaining short low-inductance bonds between the package and the die bonding pads for excellent high-frequency performance.

The tungsten-copper base of the package also serves as the ground plane for the alumina substrate that is attached on top of it. This 5 mil thick alumina substrate was deliberately kept thin to allow the physical width of the printed transmission lines to remain small. Narrow width lines are required because the pad pitch on the die is only 5.9 mil and contiguous pads are used for many of the high speed signals. Consequently, transmission-line widths greater than approximately 2 mil would be too large to permit adjacent pads on the die to be connected while maintaining acceptable cross-talk levels between adjacent transmission lines.

Both the multiplexer and demultiplexer ICs use differential signals for nearly all the high-speed data and clock signals. Consequently, coupled microstrip transmission lines can be used for each differential pair to increase the permissible transmission line density and eliminate the need for an excessively thin substrate that would increase package material and assembly costs. A balanced differential signal will excite only the odd-mode of a coupled transmission line. Consequently, only the odd-mode impedance of the line needs to be designed to be equal to the $50\,\Omega$ characteristic impedance of the system. The differential signals will see the desired $50\,\Omega$ impedance when driving the coupled lines regardless of the even-mode impedance, since the even mode will not be excited.

Coupled microstrip lines have the property that the conductor width and separation can be varied in such a way that the odd-mode impedances can be kept constant while the even-mode impedance is varied. This property can be exploited to permit the coupled microstrip lines to be tapered as they travel from the package edge to the die. Wide lines and spacings at the package edge facilitate the interface of the package to the printed circuit board, whereas narrow lines and spacings at the die are needed to interface to the 5.9 mil pitch of the die bond pads. Using this technique, a pitch of 20 mil between conductors at the package edge was tapered down to a 5.9 mil pitch at the die edge. In the process, the even mode impedance varied from $59\,\Omega$ for the widely spaced conductors at the package edge to $80\,\Omega$ for the narrower lines near the die.

Special consideration was given to the design of the coupled transmission lines as they pass through the ceramic seal-ring that forms the walls of the internal cavity of the package. At the point where the coupled microstrip lines pass through the seal-ring, a transition occurs to an embedded coupled-line microstrip geometry. Consequently, the line widths and separations need to be adjusted to account for the added alumina layer above the conductors. The seal-ring transition was simulated using the HP-EEsof Series IV Libra design suite [3]. The embedded coupled microstrip was modelled with a Libra two-conductor PCLINE2 element model that is based upon a quasi-static analysis in an enclosed region with multiple layers of a single dielectric [4].

An additional complication arose with the design of the demultiplexer package. The demultiplexer package, unlike the multiplexer with only high-speed differential signals, needs to accommodate two single-ended high-speed signals in addition to 24 differential high-speed signals. Unfortunately, a single-ended signal precludes the use of coupled-lines. Without coupled-lines, the ability to taper the line width from the package edge to the die is not possible without affecting the characteristic impedance of the line.

A $50\,\Omega$ microstrip line has a width of 4.7 mil on the 5 mil thick alumina substrate. This is too wide to interface with the 5.9 mil pitch die bond pads. As a result, the microstrip line was tapered to a 3 mil width over a 95 mil segment as the line approached the die. Consequently, the characteristic impedance increases as the width narrows to a maximum of $60\,\Omega$. This results in an inherent mismatch for the line. Simulations show the tapered line limits the return loss to no better than 15 dB above 10 GHz. Fortunately, while this is not as good as the differential coupled-line signal paths, it is sufficient for our application.

Both the multiplexer and demultiplexer ICs have numerous ground pads around the periphery of the die. These ground pads must be bonded to a low-inductance ground on the package if the IC is to operate error-free at the full 10 Gb/s data rate. Typically, a low-inductance “bounce-free" ground is obtained using a short low-impedance ground line from near the IC ground pad to a via through the substrate to the grounded copper-tungsten base. Unfortunately, this conventional approach has several problems. The 5.9 mil bond pad pitch

on the die is much narrower than the width of the smallest available via. Consequently, to make room, the via must be placed some distance from the die. Unfortunately, the tight pad pitch prevents the use of wide low-impedance lines from the die to the via to reduce the effect of the long ground path. In addition, vias are quite expensive to manufacture and so their use is discouraged in low-cost applications.

To satisfy the grounding requirements, a 6 mil wide rectangular conductive ring was etched on the substrate around the periphery of the hole for the die and the ring grounded at each of the four corners with large vias. Provided the segments of the ring between the vias are short enough not to resonate in the energy band of the signals, this technique allows any pad on the periphery of the die to be grounded by connecting it to the ring with a short bond wire. The high-speed microstrip lines are brought up perpendicular to the ground ring and then bond wires are jumpered over the ring to the die bonding pads. The total length of such a bond wire is typically no longer than 10 mil using this method, resulting in an inductance of approximately 130 pH. For extremely critical signals, the ground ring width can be thinned near the pad to permit a shorter bond wire to be used. This technique was used for the 10 GHz clock signals for both ICs to reduce the bond wire length to less than 7 mil for these critical signals.

III. Package Performance

Two experimental research prototype package designs have been fabricated. One package is designed to match the layout of the demultiplexer IC, and the other to match the multiplexer IC. In addition, for testing and integration, custom high-speed printed-circuit boards have been designed for each package using Rogers TMM-10 microwave laminate.

Measured results of the packaged demultiplexer die show an average 7% increase in maximum operating data rate compared to the on-wafer membrane-type probe test results for the same die. Maximum error-free data-rates of up to 12.5 Gb/s, limited by the internal divider circuitry, were observed for the packaged demultiplexer operating at nominal supply voltage. Similar results were obtained with the multiplexer IC. Figure 2 shows the eye diagram of the packaged multiplexer. Measured risetimes of 35–45 ps are typical for the packaged parts.

Measurements of the time-domain response and differentially excited return loss of the packaged multiplexer and demultiplexer dies have been performed for the high-speed differential leads. Custom modifications to a commercial HP 8510 network analyzer were designed and built to allow differentially excited return loss measurements to be made over a wide frequency range. In addition, measurements of the return loss of the high-speed single-ended signal paths have also been made.

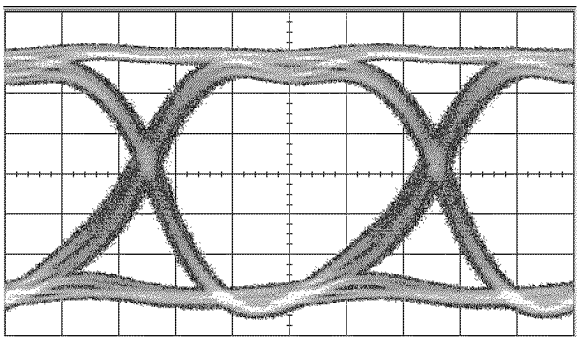

Figure 2. Measured eye diagram of the packaged multiplexer operating at 10 Gb/s. The vertical scale is 200 mV per division and the horizontal scale is 20 ps per division. The eye height is 925 mV and the eye width is 88 ps.

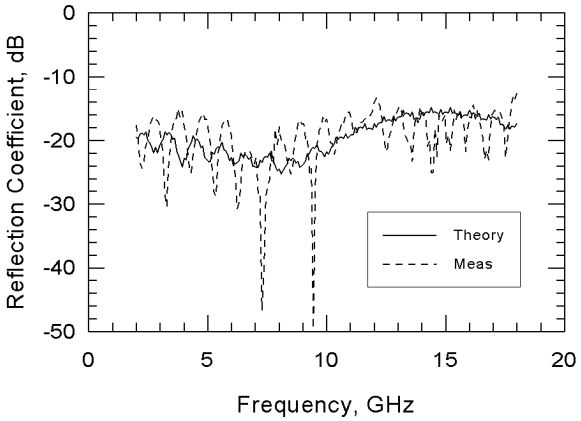

Figure 3. A comparison of theory and measured return loss for the differential 10 Gb/s data inputs of the demultiplexer package including the effects of the printed-circuit test fixture. The return loss is better than 15 dB up to 18 GHz.

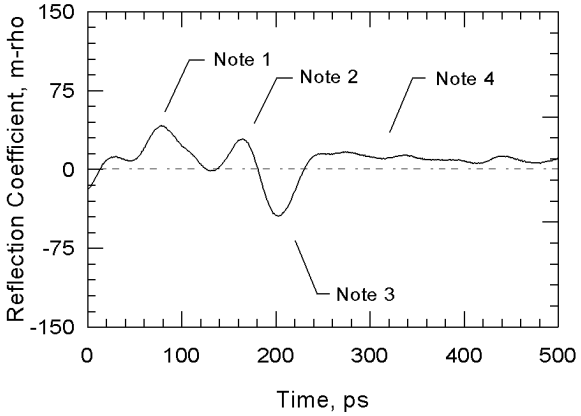

Figure 4. The measured time-domain response for the differential 10 Gb/s data inputs of the demultiplexer package. The largest reflections occur at the pcb-to-package wire bonds (1), the package seal ring (2), and the package-to-die wire bonds (3). The on-chip 50 Ω NiCr termination resistors (4) provide excellent high-frequency performance.

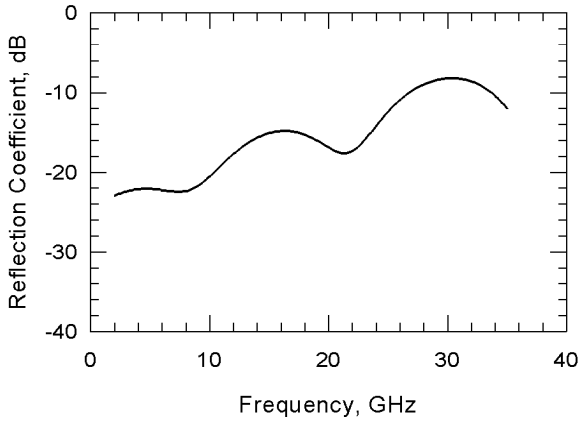

Figure 5. The theoretical return loss of the package extrapolated to 35 GHz after de-embedding the response of the test fixture. The package has better than 15 dB return loss to 24 GHz, and is still usable at frequencies up to as high as 35 GHz.

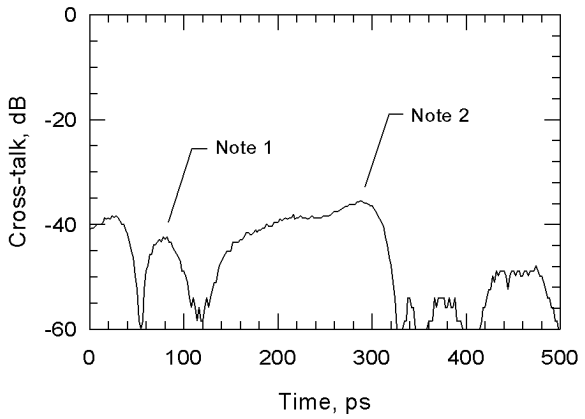

Figure 6. The measured time-domain transfer response (crosstalk) between adjacent pairs of differential data inputs of the multiplexer package. The largest source of crosstalk is at the pcb-to-package wire bonds (1) and the package-to-die wire bonds (2) of the signal paths.

Figure 3 shows a comparison of theoretical and measured return loss for the differential 10 Gb/s data input of the demultiplexer package. Good agreement is observed between theory and measurement. Figure 4 shows the time-domain response of the same signal path using a 30 ps pulse. After de-embedding the printed-circuit board response, the package seal-ring and wire-bonds are the only source of significant reflections. Figure 5 shows the theoretical return loss of the package extrapolated to 35 GHz obtained after de-embedding the printed-circuit board lines from the measured data and then extrapolating the resulting model to 35 GHz. Figure 6 shows the time-domain signal crosstalk between adjacent differential pairs measured using a differential TDT pulse. Crosstalk better than -35 dB was measured along the package signal path. A comparison of measured and theoretical return loss for one of the two single-ended signal paths of the demultiplexer package is shown in Figure 7.

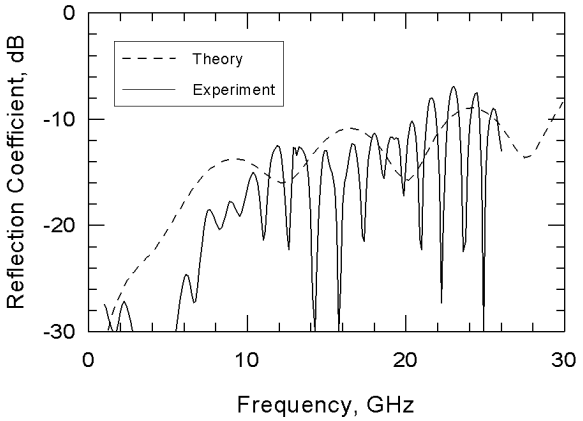

Figure 7. Theory and measurement of the return loss for a single-ended line from 1 to 26 GHz. The simulation results, confirmed by measurement, show that the tapered line limits the return loss to no better than 15 dB above 10 GHz.

IV. Conclusion

Experimental research prototype packages with up to 26 10 Gb/s I/O ports were designed for two GaAs telecom ICs. The packages provide excellent thermal dissipation and high-speed characteristics. Usable bandwidth of the packages extends up to 35 GHz demonstrating that the package need not be the limiting factor in large I/O count, high-speed digital systems. The packaged parts have been installed into Tektronix designed STS-192 transmitter and receiver circuit packs, and are currently being field tested as part of an experimental OC-192 testbed in Austin Texas. High-speed measurements of the system containing the packaged multiplexer and demultiplexer ICs have been made and extended error-free operation at 10 Gb/s has been verified.

References

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